Dynamic Behaviors of Grid-Connected Inverters During Voltage Dips

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Abstract

The task in this traineeship is to simulate a grid-connected inverter and observe the support of the inverters on the point of common coupling (PCC) during dips. In this article, the principle of a grid inverter and its control strategy are introduced. When the inverter is proved with high performance, several of them are distributed in different feeders and different dips conditions are simulated to see the voltage variations compared to a low voltage bus line without inverters. Simulation results show that the inverters can indeed help increase the voltage in the PCC during dips.

1. Introduction

Photovoltaic (PV) power are highly demanded in recent years. With more and more inverters connected to the grid, the power quality issues are concerned when a large amount of inverters inject power to the grid. On the other hand, the grid may also affect the distributed generators if the grid is already polluted. It requires the distributed devices, such as wind generators and PV systems, to be capable of when the grid voltage temporarily reduces in one, two or three phases due to a fault or load change in the grid.

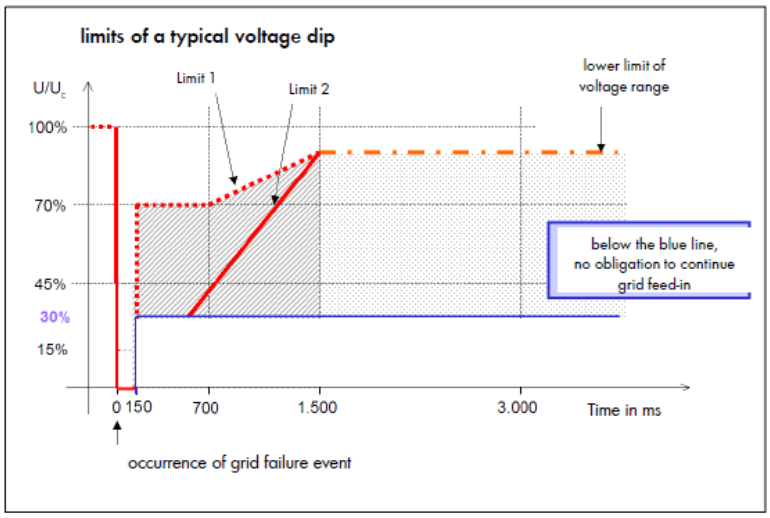

Figure 1 Limits of a Typical Voltage Dip

There are some standards for the low voltage ride through (LVRT). Figure 1 gives a standard from German BDEW technical guideline for generating plants connected to the medium voltage grid, in June

2008. It has three states during the dip as continuous and stable operations above limit 1; may disconnect in accordance with grid operator between limit 1 and limit 2; and may disconnect from the grid below limit 2 and below the blue line.

The inverters should work fulfilling such requirements. Besides, the inverters could also raise the grid voltage itself during the dips, which is helpful to the LVRT. In this article, an inverter with low harmonics or inrush currents is established in MATLAB to observe such phenomena above. Usually digital inverters are widely used in the industrial to achieve such control illustrated in Fig 1. However, in order to simplify the algorithms, an analogue control is used in this simulation and all the tested dips values are above 0.3pu.

2. The Inverter

2.1 The Topology of a Single-phase Full-bridge Inverter

The topology of single-phase full-bridge PWM inverters is shown in figure 2. E_{dc} is the DC bus voltage. A full-bridge inverter connects the DC bus and the LC filter by pulse width modulation (PWM) control. L_f and C_f represent the output filter inductance and capacitance, while r is the resistance of the inductor. The impedance of load is shown as Z.

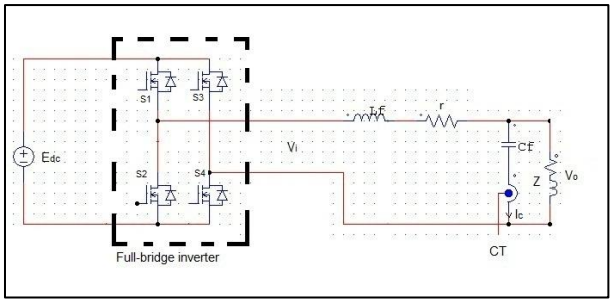

Figure 2 Topology of Single-phase Full-bridge PWM Inverter

In this simulation, voltage and output current are two feedbacks to maintain the high performance of the inverter.

2.2 Physical System of an Inverter

When the switches are considered as ideal components, we may describe the switch function as

$$S = \begin{cases} 1 \ when \ S_1 \ and \ S_4 \ are \ switched \ on \ and \ S_2 \ and \ S_3 \ swtiched \ off \\ -1 \ when \ S_1 \ and \ S_4 \ are \ switched \ off \ and \ S_2 \ and \ S_3 \ swtiched \ on \end{cases}.$$

Under the ideal conditions with no dead time, the signals of S_1 and S_4 are opposite from those of S_2 and S_3. Therefore, V_i is a bipolar pulse voltage and its value is given by

$$V_i = S \cdot E_{dc} \quad .$$

The SPWM (Sinusoidal Pulse Width Modulation) bridge modulates the error signal with high frequency bipolar triangle wave. This is several orders of magnitude to the fundamental output frequency. By this way we may regard the average value of V_i in each switch cycle as an instantaneous voltage in low frequency. Then, we may deduce the average value of V_i by figure 3 where v_m is the modulating signal, and V_{tri} is the amplitude of the triangle wave.

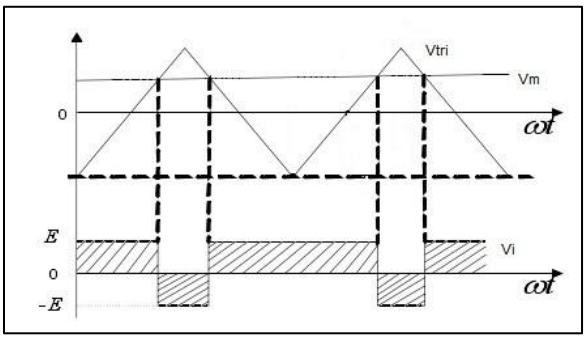

Figure 3 The Relationship between the Driving Signals and the Input Signals

From $\overline{V_i} = E_{dc}\frac{V_{tri}+v_m}{2V_{tri}} - E_{dc}\frac{V_{tri}-v_m}{2V_{tri}} = E_{dc}\frac{v_m}{V_{tri}}$, we can conclude that the average value of Vi in a switch cycle is in proportion to the modulation voltage. When the input voltage and the triangle wave are constant, the shape of $\overline{V_i}$ is the same with the modulating signals. Therefore, the desired output wave is achieved by using proper modulating signals.

Besides the desired voltage waveform, this output may also include high frequency noise at switching frequency(f_s) and even higher harmonics. The LC filter can deal with this problem. The corner frequency of the LC filter is usually chosen to be far below f_s in order to obtain low total harmonic distortion (THD) in the output waveform.

2.3 Controller Strategy of the Inverter

In this simulation, an active/reactive power control method is adopted. Since the voltage from the DC side is usually the output of the boost converter with MPPT control, its voltage should be stable, as well as its output power is known. Thus, the DC voltage of the inverter is assumed to be constant and the power that it can provide is used to control the output current. According to the power and voltage, we can calculate the current, which is compared with the feedback to achieve the control. In the AC system, it is necessary to decouple the vector to control active and reactive power separately. Considering the fact that the inverter should provide stable power during unbalanced conditions, it is hard to control all

three phases together by a three-phase inverter. Thus, we just design a single-phase inverter and parallel them together.

In this part, the strategy is introduced in the following steps: direct/quadrant axis; decouple the interference between direct and quadrant axis; parameters design.

2.3.1 dq Axis

As we know the amplitudes and phases of the voltage and current, we need to transfer it to αβ bases, then to dq bases. This deduction is shown below.

$i_{o\alpha}$ = $i_o \sin(\omega t+\phi)$ (ϕ is the power factor)

$i_{o\beta}$ = $i_o \sin(\omega t+\phi-pi/2)= -i_o \cos(\omega t+\phi)$

$u_{o\alpha} = u_o \sin(\omega t)$

$u_{o\beta} = u_o \sin(\omega t-pi/2)= -u_o \cos(\omega t)$

Then,

$i_{od}= i_o \cos\phi = i_{o\alpha} * \sin \omega t - i_{o\beta} * \cos\omega t$

$i_{oq}= i_o \sin\phi = i_{o\alpha} * \cos \omega t + i_{o\beta} * \sin\omega t$

$u_{od}= u_o = u_{o\alpha} * \sin \omega t - u_{o\beta} * \cos\omega t$

$u_{oq}= 0 = u_{o\alpha} * \cos \omega t + u_{o\beta} * \sin\omega t$

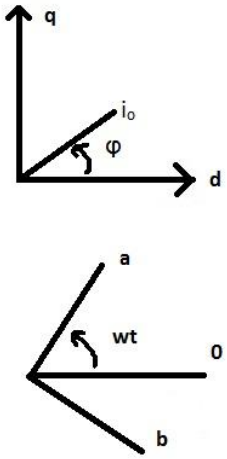

Figure 4 voltage in dq and αβ axis

This way, we can deduct the transfer matrix as followings.

αβ=>dq matrix	dq=> αβ matrix
[sin ωt, -cos ωt;	[sin ωt, cos ωt;
cos ωt, sin ωt]	-cos ωt, sin ωt]

2.3.2 Decouple the Interference

From Fig 5, we may find that

$V_{ref} = I_L * j\omega L + V_{grid}$

$I_L = I_g + I_C$

$I_C = j\omega C * V_{grid}$.

Thus, we may conclude that

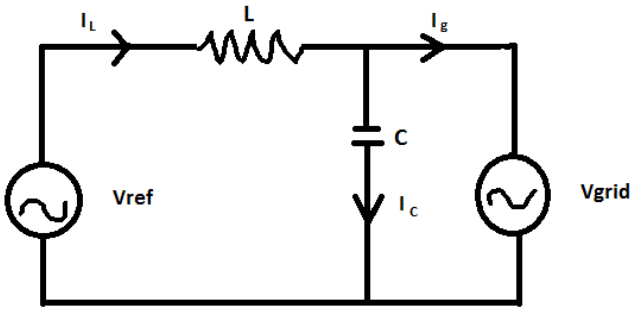

Figure 5 Model for the Inverter and the Grid

$V_{ref} = j\omega L(j\omega C * V_{grid} + I_g) + L*dI/dt + V_{grid} = (1-\omega^2 LC)*V_{grid} + j\omega L*I_g + L*dI/dt$

Then

$V_{ref,d} = (1-\omega^2 LC)*V_{grid,d} + j\omega L*j*I_{g,q} + L*dI_d/dt$ => $V_{ref,d} = (1-\omega^2 LC)*V_{peak} - \omega L*I_{g,q} + L*dI_d/dt$

$j*V_{ref,q} = (1-\omega^2 LC)*j*V_{grid,q} + j\omega L*I_{g,d} + L*dI_q/dt$ => $V_{ref,q} = \omega L*I_{g,d} + L*dI_q/dt$

2.3.3 Parameters Design

With the decoupled system, we can precisely control the inject current shown as Fig 6.

The PI parameter can be calculated by equations below:

$V_{ref,d} = V_{pi,d} - \omega L*(I_q) + V_{peak}$; $V_{ref,q} = V_{pi,q} + \omega L*(I_d)$.

$V_{pi,d} = k_p*(i_{ref,d} - i_d) + k_i\int(i_{ref,d} - i_d)dt$

$V_{pi,q} = k_p*(i_{ref,q} - i_q) + k_i\int(i_{ref,q} - i_q)dt$

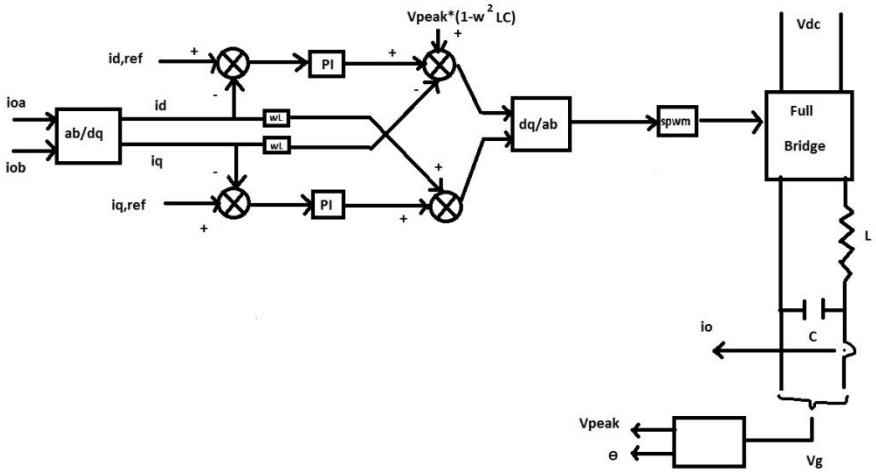

Figure 6 Control Strategy

Combining equations above, we can find that

$L*dI_d/dt = V_{pi,d} = k_p*(i_{ref,d} - i_d) + k_i\int(i_{ref,d} - i_d)dt$

$L*dI_q/dt = V_{pi,q} = k_p*(i_{ref,q} - i_q) + k_i\int(i_{ref,q} - i_q)dt$

Thus,

$L*d^2I_d/dt^2 + k_p*di_d/dt + k_ii_d = k_i*i_{ref,d}$

$L*d^2I_q/dt^2 + k_p*di_q/dt + k_ii_q = k_i*i_{ref,q}$

This is a second-order ordinary differential equation. If the damping coefficient is set as half cycle (10ms), we may calculate that

$1/\tau = (-k_p \pm sqrt(k_p^2 - 4*L*k_i))/2L$

We select $k_p^2 - 4*L*k_i = 0$ and $k_p/2L = 0.707/0.01s$ (the time constant is set as 0.01s).

By this way, kp is 1.7 and ki is 60. In practical use, in order to get a faster response, kp is 3.2 and ki is 240. Here the inductance is chosen as 12mH. The filter corner frequency should be 1/10 of the switching frequency as 10kHz. By this way, we can find that the filter capacitance is 2.11μF.

The DC bus line should be adjusted according to the output voltage as well as power. When the power is quite large, the decoupled vector I*jωL will become much higher than the grid voltage, which requires the DC bus a high voltage. In practical use, there are usually lots of PV inverters connected to the LV bus. However, the simulink software has limited memory which cannot calculate with too many inverters. Here, we just use 4 inverters with large output power to stand for the normal conditions.

The power of each inverter in single phase is 150kW, which leads the DC voltage to thousands of volts. The reference current could be calculated with the injecting power. During the dips, the voltage would be small and the current would be very large. In order to avoid large inrush current, a current limit is added as 120% nominal current. With several trials, the inverter could finally work with high performance in single-phase and three-phase conditions.

3. Inverters in the Grid

As shown in Fig 7, it is assumed that the LV bus line, connected to the MV side with a MV/LV transformer, having 4 feeders to the inverters and loads. In the MV side, the voltage source provides 10 kV voltage and contains 1% of fifth and seventh harmonics. The transformer is a 10kV/0.4kV in the structure of delta/star with power capacity of 630kVA. In the LV side, each inverter provides 300kW in total and the load in each feeder consumes 360kW. Those feeders are connected with a 100-metre long cable. The model of the cables' impedance is shown in Fig 8. The resistance in each phase is 5mΩ and inductance is 11μH. The capacitance in each side is 20nF.

In this simulation, the voltage at the PCC is observed compared with no inverter conditions.

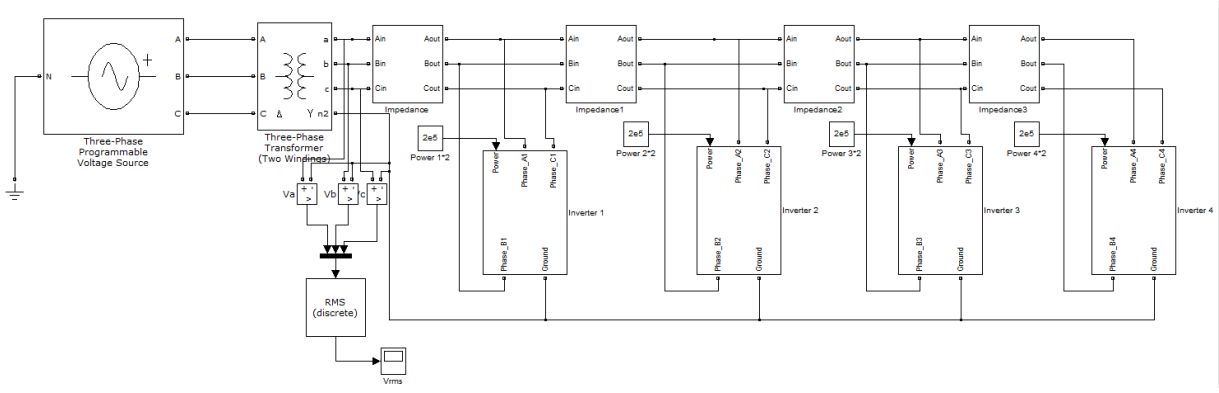

Figure 7 Inverters Connected to the Feeders in the LV side

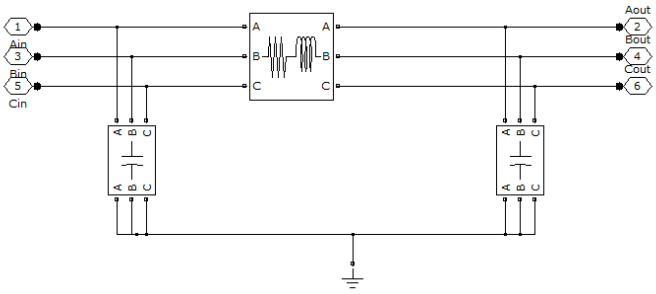

Figure 8 Model of a Cable Impedance

4. Simulation Results and Analyses

In this simulation, different dips conditions are introduced. Dips in one phase, two phases and all three phases with dip depth from 0.1 to 0.7 are all tested taking place at 0.25s in each simulation. Since most the waveforms are similar, this report only shows one graph of waveforms in similar conditions. The others are recorded as values.

4.1 Dips in Single Phase

In this simulation, a dip depth with magnitude of 0.7pu is taken as an example. The voltage and current waveforms, magnitudes, power and reactive power injected by the inverter, and the root mean square (rms) value of voltage at PCC are separately shown.

In Fig 9, the waveform is shown of the voltage and inverter output current at feeder 1 between 0.2 to 0.3s. The waveform is quite good with voltage THD lower than 1.5% and current lower than 0.5%.

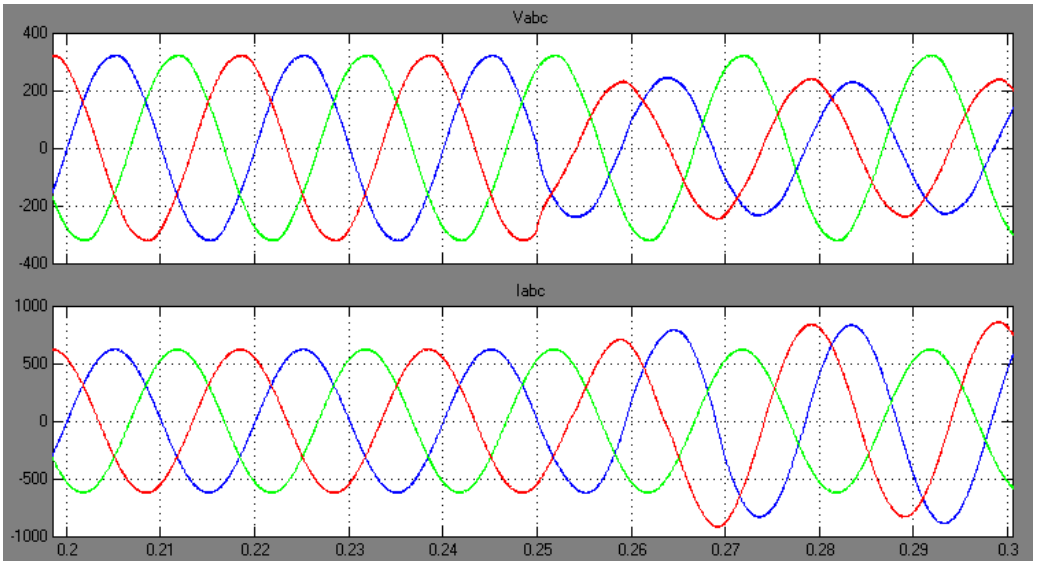

Figure 9 Voltage and Current Waveforms in Feeder 1

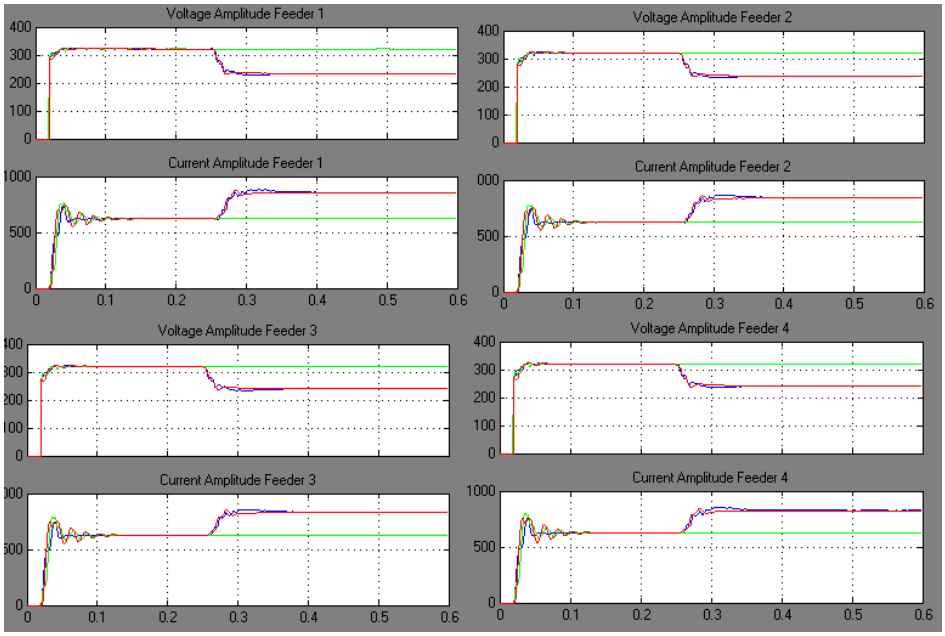

Figure 10 Amplitude of V&I in Each Feeder

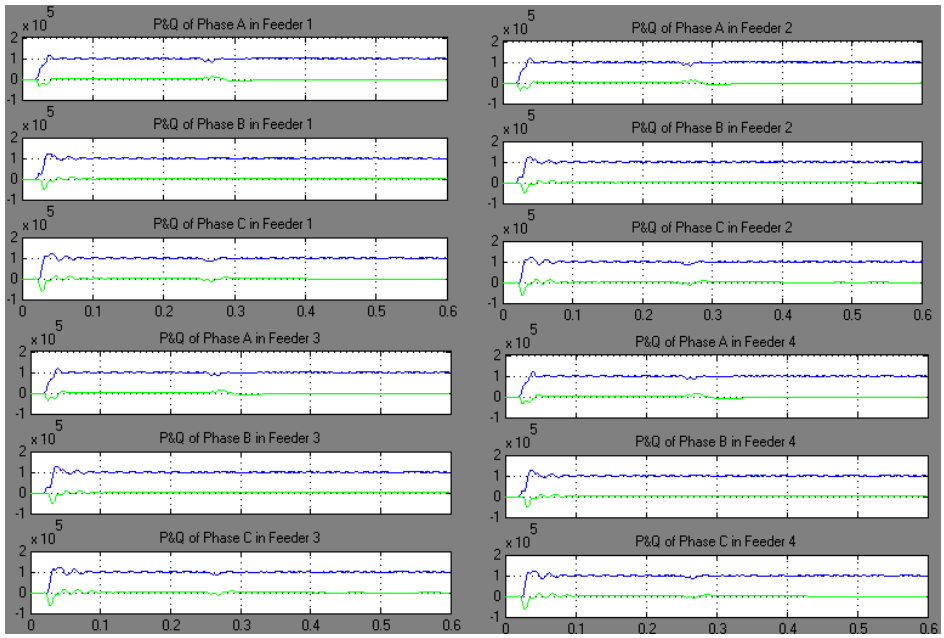

Figure 11 Active/Reactive Power in Each Feeder

From Fig 10, we may find that the single-phase voltage dip after the Δ/Y transformer has a lower amplitude in two phases. The current is increasing to maintain the output power as constant as 100kW per phase in Fig 11.

The rms value of voltages at PCC is shown in Fig 12. It indicates that after the dip, voltage in Phase B is the same as before, while that in Phase A and C suffers from the dips. Detailed values and the rest rms voltage values at PCC are recorded in Table 1, compared with the same conditions only without inverters.

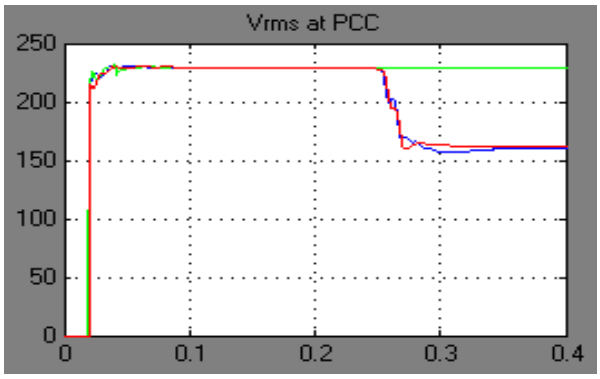

Figure 12 rms Value of Voltage at PCC

Table 1 Voltage at PCC during single-phase dips

Dip depth in one phase (pu)	rms value of voltage at PCC with (without) Inverters Connected / V			Increase Value / V		
	Phase A	Phase B	Phase C	Phase A	Phase B	Phase C
0.3	161.3(146.0)	228.9(214.4)	161.3(146.0)	15.3	14.5	15.3
0.4	170.2(154.6)	228.9(214.4)	170.2(154.6)	15.6	14.5	15.6
0.5	179.5(163.7)	228.9(214.4)	179.5(163.7)	15.8	14.5	15.8
0.6	188.9(173.3)	228.9(214.4)	188.9(173.3)	15.6	14.5	15.6
0.7	198.6(183.2)	228.9(214.4)	198.6(183.2)	15.4	14.5	15.4
0.8	208.5(193.3)	228.9(214.4)	208.5(193.3)	15.2	14.5	15.2
0.9	218.6(203.8)	228.9(214.4)	218.6(203.8)	14.8	14.5	14.8

From Table 1, we may find that with the currents injected by the inverters, it will increase the voltage at PCC of the LV bus. Phase A and C suffer from the dips, and it has improved by about 15V. When the voltage's amplitude drops from 0.9pu to 0.5pu, the support is increasing since the smaller with the voltage, the larger with the inverter output current to maintain the power constant. When the voltage is lower than 0.4pu, the support is decreasing a bit.

4.2 Dips in Two Phases

In this simulation, there are dips in two phases in the MV side, and after the Δ/Y transformer there is a deep dip in Phase A and two small dips in Phase B and Phase C. The waveform under the dips as 50% in MV side is shown below.

The waveforms of voltage and current in feeder 1 is shown in Fig 13. The voltage in Phase A drops more than that in Phase B and C, while the current in Phase A is increasing more. The voltage THD is less than 1.5%, while the current THD is less than 0.5% in steady state.

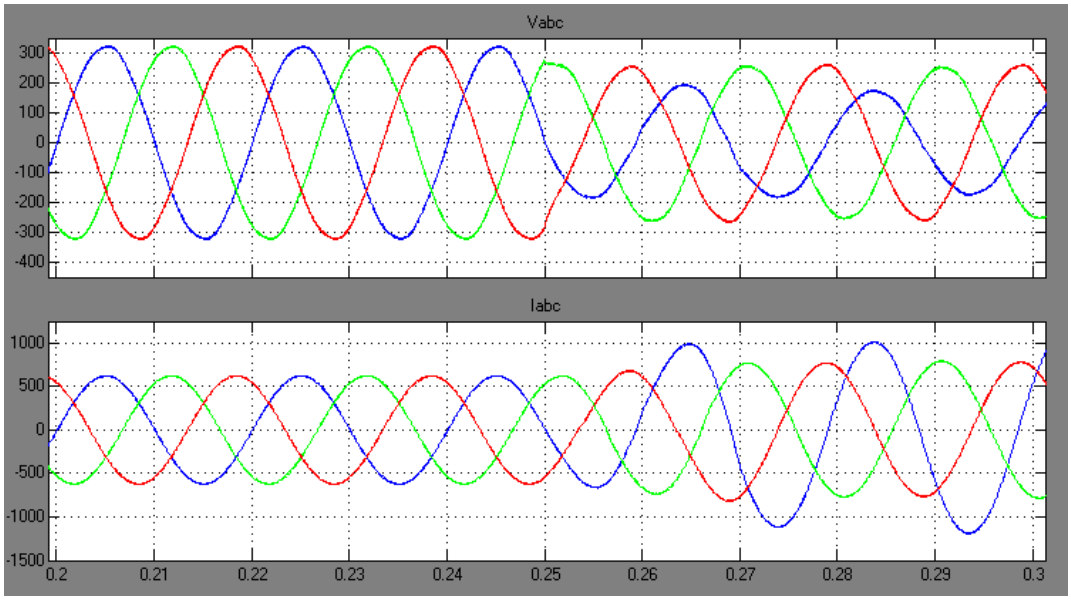

Figure 13 Voltage and Current Waveforms in Feeder 1

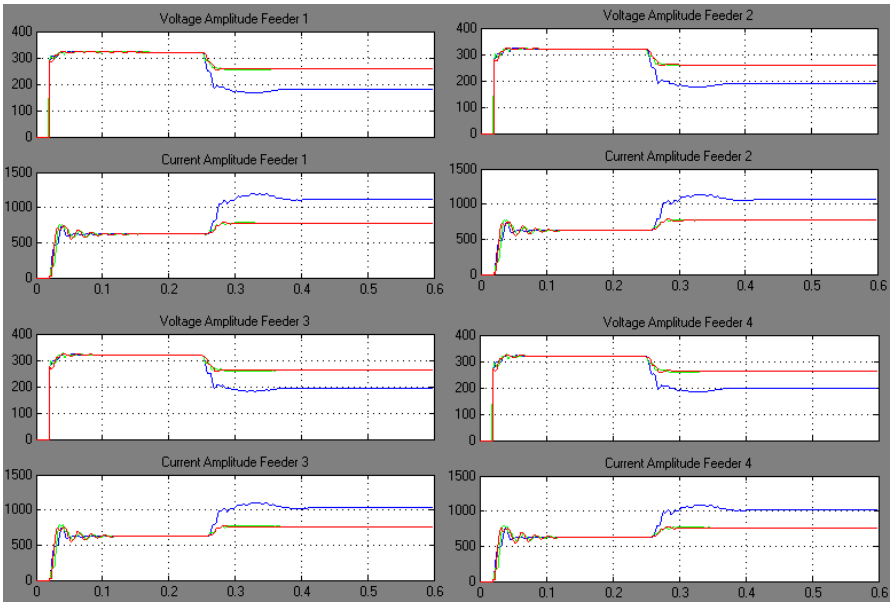

Figure 14 Amplitude of V&I in Each Feeder

From Fig 14, it is observed that the voltage and current get stable very quickly in all feeders. The active power and reactive power are not shown here, since it is almost constant all the time like Fig 11.

The rms values of voltage at the PCC are listed in Table 2. There is always an increase in the voltage during the dips. The increase is about 15V when the voltage is larger than 120V. When it is lower than 120V, the increase becomes smaller. This might be due to the unbalanced loads. And when the voltage drops to 0.3 or 0.4pu, there is a large distortion in Phase A. Perhaps at this moment, the grid voltage is

too small and the injected current is so large that it affects the performance of phase lock loop (PLL), and then affect the total performance of the inverter. At this time, the inverter should disconnect from the grid.

Table 2 Voltage at PCC during dips in two phases

Dip depth in one phase (pu)	rms value of voltage at PCC with (without) Inverters Connected / V			Increase Value / V		
	Phase A	Phase B	Phase C	Phase A	Phase B	Phase C
0.3	Serious Distortion in Phase A					
0.4	Serious Distortion in Phase A					
0.5	118.5(107.2)	179.5(163.7)	179.5(163.7)	11.3	15.8	15.8
0.6	144.0(128.6)	188.9(173.3)	188.9(173.3)	15.4	15.6	15.6
0.7	166.0(150.1)	198.6(183.2)	198.6(183.2)	15.9	15.4	15.4
0.8	187.3(171.5)	208.5(193.3)	208.5(193.3)	15.8	15.2	15.2
0.9	208.1(192.3)	218.6(203.8)	218.6(203.8)	15.8	14.8	14.8

4.3 Dips in Three Phases

In this simulation, three phases dips are involved in the MV side, and after the transformer there is a balanced dips for all three phases. The waveform under the dips as 60% of nominal voltage is shown below.

The waveforms of voltage and current in feeder 1 is shown in Fig 15 The magnitudes of voltages and currents are the same among three phases. The VTHD is less than 1.5% and the CTHD is lower than 0.4%.

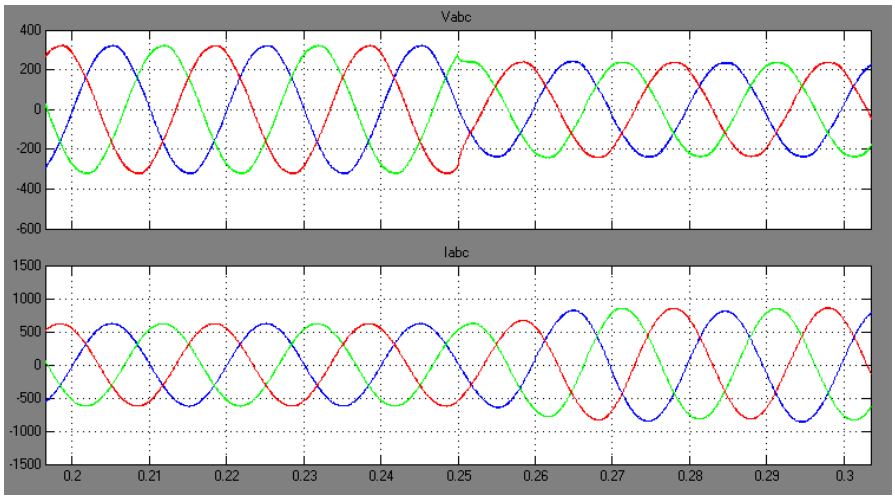

Figure 15Voltage and Current Waveforms in Feeder 1

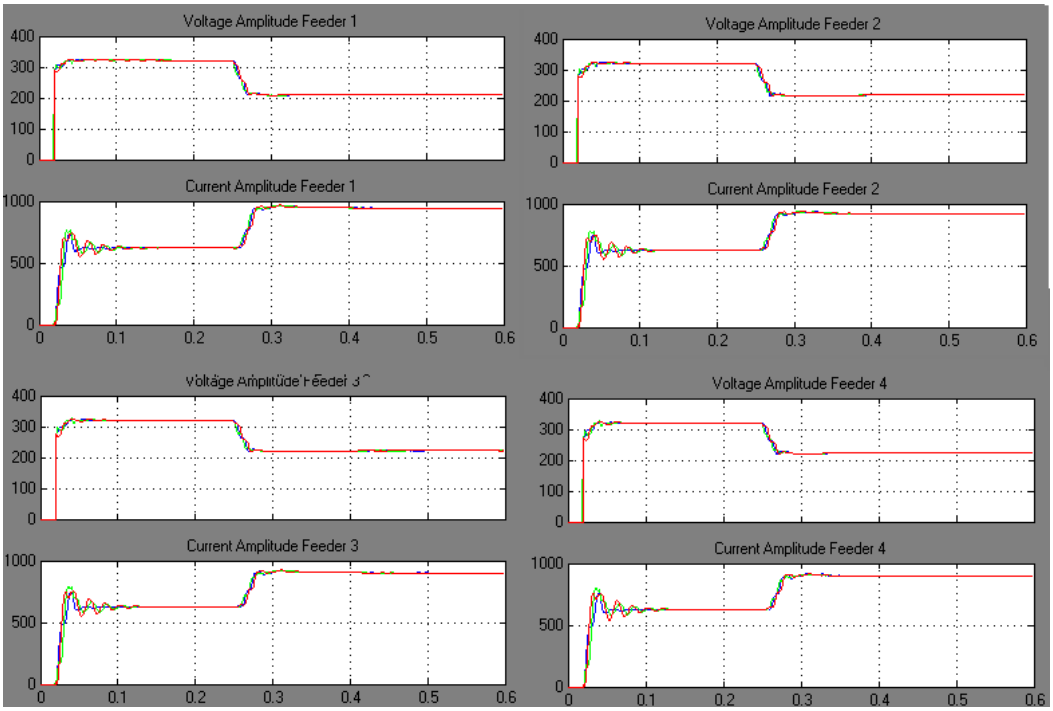

Figure 16 Amplitude of V&I in Each Feeder

In Fig 16 are shown the amplitudes of voltage and current among 4 feeders. The voltage drops in all three phases with the same amplitude and so increases the current. We can see that the response is also fast in this condition.

The rms values of the voltage at PCC are recorded in Table 3. Since the three phases are balanced, it is recorded together in a mean value. A nominal state is also added as a reference. Simulation results show that the inverter could make a contribution to the voltage increase during dips except when the voltage is lower than 120V. This is the same phenomenon as shown in Table 2. The support by the inverter is larger if the grid voltage is lower for most cases. However, if the grid voltage is too low, there might be distortions in the voltage due to the injected currents and the non-resistive impedance of the cables.

Table 3 Voltage at PCC during dips in three phases

Dip depth in two phases (pu)	rms value of PCC with inverters connected / V	Voltage at PCC without inverters / V	Increase / V
0.3	Serious Distortion in Three Phases		
0.4	Serious Distortion in Three Phases		
0.5	118.4	107.2	11.2
0.6	144	128.6	15.4
0.7	166.1	150.1	16
0.8	187.2	171.5	15.7
0.9	208.1	192.3	15.8
1.0	228.9	214.4	14.5

4.4 PV Inverters Working in Half Nominal Power

If the inverter is not providing the nominal power, the current could be lower than the nominal ones. By this way, there will be a lower increase in the voltage during the dips and this would cause a smaller distortion. The result with half nominal power injected is simulated.

The waveforms are similar, and here only presents the record of the rms values of the voltage at PCC, as listed in Table 4. We may find that the support is also a bit larger when the grid voltage is lower for most cases. Also in this condition, the inverter works well when the grid voltage is 0.4pu rather than that in nominal conditions. The only disadvantage is that this support is less than nominal state, which is obvious that the support is relevant to the injected power.

Table 4 Voltage at PCC during dips in two phases with inverters providing half power

Dip depth in one phase (pu)	rms value of voltage at PCC with (without) Inverters Connected / V			Increase Value / V		
	Phase A	Phase B	Phase C	Phase A	Phase B	Phase C
0.3	Serious Distortion in Phase A					
0.4	96.3(85.8)	164.8(154.6)	164.8(154.6)	10.5	10.2	10.2
0.5	118.6(107.2)	173.6(163.7)	173.6(163.7)	11.4	9.9	9.9
0.6	139.7(128.6)	182.9(173.3)	182.9(173.3)	11.1	9.6	9.6
0.7	160.4(150.1)	192.4(183.2)	192.4(183.2)	10.3	9.2	9.2
0.8	181.1(171.5)	202.2(193.3)	202.2(193.3)	9.6	8.9	8.9
0.9	201.9(192.3)	212.4(203.8)	212.4(203.8)	9.6	8.6	8.6

4.5 Analyses

From Section 4.1 to 4.4, we can find that the inverters work well in both transient and steady states. It injects low harmonics into the grid, and the response is fast. The support by the inverters could be seen from Table 1 to Table 4. When the grid voltage is not too low (above 120V), the support is larger with a lower grid voltage, which is as the predict we make. When the voltage is lower than 120V, this support is not as large as before probably due to the unbalanced loads. When the voltage is lower than 100V, it might be distorted and cannot reach the stable state. This is depended on both grid voltage and the injected power. The support value is related to the power of inverters, the impedances of the cable and the transformer, as well as the load. It could be considerable if proper designed.

5. Conclusion

The inverter introduced in this report is proved capable to work with high performance in MATLAB. Using this model in the low voltage bus, we find that grid-connected inverters could help increase the voltage for about 10 to 15V at PCC during dips. Inverters using in this model adopts a simple analogue

control, while digital inverters are more popular in practical use to achieve more flexible controls. With advanced digital inverters and proper arrangement, it will support with the grid during dips.

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